IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.; WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY TECHNOLOGY CO., LTD.; TIANMA MICROELECTRONICS CO. LTD.; AND VISIONOX TECHNOLOGY, INC.
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Case No. IPR2023-00941
U.S. Patent No. 7,414,599

PETITIONER'S NOTICE OF APPEAL

Pursuant to 28 U.S.C. § 1295(a)(4)(A), 35 U.S.C. §§ 141(c), 142, and 319, and 37 C.F.R. §§ 90.2(a), 90.3, and Federal Circuit Rule 15(a)(1), Mianyang BOE Optoelectronics Technology Co., Ltd., Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd., Tianma Microelectronics Co. Ltd., and Visionox Technology, Inc. ("Petitioner") provides notice that it appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision of the Patent Trial and Appeal Board ("Board") entered December 6, 2024 (Paper 68), and from all underlying and related orders, decisions, rulings, institutions, and opinions regarding U.S. Patent No. 7,414,599 ("the '599 patent") at issue in *Inter Partes* Review No. IPR2023-00941. This notice of appeal is timely filed because it is filed within 63 days of the December 6, 2024 Final Written Decision.

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), the expected issues on appeal include, but are not limited to: the Board's determination that Petitioner did not establish that claims 1-18 of the '599 patent are unpatentable and all other issues decided adversely to Petitioner in any orders, decisions, rulings, or opinions in this proceeding.

Pursuant to 35 U.S.C. § 142 and 37 C.F.R. § 90.2(a), a copy of this Notice is being filed with the Director of the United States Patent and Trademark Office and with the Patent Trial and Appeal Board. In addition, a copy of this Notice and the

required docketing fees are being filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit via CM/ECF.

Dated: February 6, 2025

Respectfully submitted,

/ Travis Jensen /

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CERTIFICATE OF SERVICE AND FILING

I hereby certify that on February 6, 2025, in addition to being filed and served electronically through the Patent Trial and Appeal Board's P-TACTS System, this NOTICE OF APPEAL was filed with the Director of the United States Patent and Trademark Office via Priority Mail Express at the following address:

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

I also hereby certify that on February 6, 2025, this NOTICE OF APPEAL and the requisite docketing fees were filed with the Clerk's Office of the United States Court of Appeals for the Federal Circuit vis CM/ECF.

I also hereby certify that on February 6, 2025, this NOTICE OF APPEAL was served via electronic mail to the following counsel at the addresses designated for service by Petitioner:

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO. LTD., WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY TECHNOLOGY CO., LTD., TIANMA MICROELECTRONICS CO. LTD, and VISIONOX TECHNOLOGY, INC.,
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.,
Patent Owner.

IPR2023-00941
Patent 7,414,599 B2

Before JAMESON LEE, TERRENCE W. MCMILLIN, and JOHN A. HUDALLA, *Administrative Patent Judges.*

LEE, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claim Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

We instituted an *inter partes* review of claims 1–18 ("challenged claims") of U.S. Patent No. 7,414,599 B2 (Ex. 1001, "the '599 patent") owned by Samsung Display Co., Ltd. ("Patent Owner"). Paper 12 ("Decision to Institute" or "Inst. Dec."). We have authority to conduct this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. We determine that Mianyang BOE Optoelectronics Technology Co., Ltd., Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd., Tianma Microelectronics Co., Ltd., and Visionox Technology, Inc. (collectively, "Petitioner") have not proved by a preponderance of the evidence that any of claims 1–18 of the '599 patent is unpatentable.

A. Background

Petitioner filed a Petition requesting an *inter partes* review of the challenged claims pursuant to 35 U.S.C. §§ 311–319. Paper 1. Patent Owner filed a Preliminary Response. Paper 9 ("Prelim. Resp.").

The Decision to Institute was entered on December 15, 2023. Paper 12. Thereafter, Petitioner filed a Motion to Submit Supplemental Information seeking to submit three items, including a 35-page supplemental declaration (Ex. 1019) of Petitioner's expert, Daniel Foty, Ph.D. Paper 18. Patent Owner opposed the motion. Paper 19. We denied the Motion to Submit Supplemental Information and determined that the proposed supplemental information proceeded in a new direction and deviated from Petitioner's positions in the Petition by including new opinions regarding transistor 3612 in Kimura's Figure 36 embodiment. Paper 27, 9–10. We stated that "[t]he proposed supplemental declaration changes Petitioner's

theory of obviousness." *Id.* at 11. Petitioner did not seek rehearing of that denial.

Patent Owner filed a confidential Response (Paper 33, "PO Resp."); Petitioner filed a Reply (Paper 41, "Reply"); and Patent Owner filed a Sur-reply (Paper 45, "Sur-reply"). Patent Owner also filed a public version of its Response which includes redactions. Paper 32.[1]

Petitioner filed a Motion to Exclude Exhibits 2018, 2021–2043, 2047, 2049, 2051, 2052, and 2054, as well as paragraphs 136 and 138–144 of Exhibit 2008. Paper 59. Patent Owner filed an Opposition (Paper 61) to the Motion, and Petitioner filed a Reply (Paper 63) to that Opposition.

Patent Owner filed a Motion to Exclude Exhibit 1003 and 1029. Paper 58. Petitioner filed an Opposition (Paper 60) to that Motion, and Patent Owner filed a Reply (Paper 62) to that Opposition.

Petitioner filed a First Motion to Strike directed to portions of the Patent Owner Response that allegedly incorporate by reference material from Exhibits 2018, 2047, 2051, and 2052. Paper 37. Patent Owner filed an Opposition (Paper 38) to that Motion and Petitioner filed a Reply (Paper 39) to that Opposition.

Petitioner filed a Second Motion to Strike directed to arguments in Patent Owner's Sur-reply and Exhibit 2054 cited therein. Paper 46. Patent

[1] Patent Owner filed an Unopposed Motion to Seal and for Entry of Protective Order. Paper 31. We granted Patent Owner's Motion to Seal and granted-in-part and denied-in-part Patent Owner's Motion for Entry of Protective Order. Paper 55. A protective order governing the handling of confidential information in this proceeding has been entered. Paper 54.

Owner filed an Opposition (Paper 47) to that motion and Petitioner filed a Reply (Paper 50) to that Opposition.

An oral hearing was held on September 16, 2024. The hearing transcript has been entered as Paper 67.

We determine that Petitioner has not proven by a preponderance of the evidence that any of claims 1–18 of the '599 patent is unpatentable.

B. Real Parties in Interest

Petitioner identifies Mianyang BOE Optoelectronics Technology Co., Ltd. (BOE"), Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd., Tianma Microelectronics Co. Ltd., and Visionox Technology, Inc., and their subsidiaries as real parties in interest. Pet. 95. Patent Owner identifies only itself as the real party in interest. Paper 7, 2.

C. Related Matters

Patent Owner identifies the following litigations involving the '599 patent as related matters:

1. *Certain Active Matrix Organic Light-Emitting Diode Display Panels And Modules For Mobile Devices, and Components Thereof*, Inv. No. 337-TA-1351 (USITC);

2. *Samsung Display Co., Ltd. v. BOE Technology Co., Ltd.*, Case No. 2-23-cv-00309 (E.D. Tex.).

Paper 7, 2. Petitioner identifies the same investigation before the International Trade Commission, i.e., No. 337-TA-1351, as a related matter. Pet. 95.

D. The '599 Patent

The '599 patent issued on August 19, 2008, from Application No. 10/886,014, filed July 6, 2004, and claims priority to KR 10-2003-0045610, filed July 7, 2003. Ex. 1001, codes (21), (22), (30), (45).

The '599 patent is directed to a pixel circuit in an organic light emitting device, which self-compensates the threshold voltage of a driving transistor. Ex. 1001, code (57). The '599 patent describes a problem with preexisting organic light emitting devices, i.e., nonuniformity from pixel to pixel caused by a variation of the threshold voltage of the driving transistor in each pixel circuit, which leads to a difference in the current flowing through the electroluminescent element in each pixel circuit. *Id.* at 1:38–50.

The pixel circuit of the '599 patent includes an electroluminescent element for emitting light in response to an applied driving current, as well as a number of transistors and a capacitor. *Id.* at code (57). Figure 3 of the '599 patent, annotated by Petitioner (Pet. 7), is reproduced below:

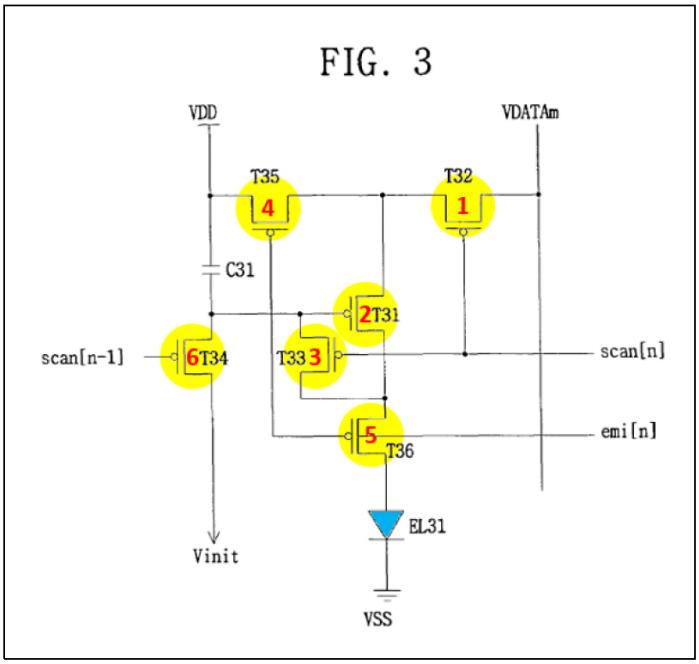


Figure 3 illustrates a pixel circuit according to one embodiment of the '599 patent. Ex. 1001, 5:65–67. Petitioner highlights transistors T32, T31, T33, T35, T36, and T34 in yellow and numbers them as 1, 2, 3, 4, 5, and 6, respectively, and highlights light-emitting element EL31 in blue. Pet. 7.

Transistor T32 switches data signal voltage VDATAm, applied to the associated data line, in response to current scan line signal SCAN[n] applied to the associated scan line. Ex. 1001, 6:24–27. Transistor T31 supplies a driving current to electroluminescent device EL31 in response to the data signal voltage from transistor T32. *Id.* at 6:27–31. Transistor T33 compensates for the threshold voltage of transistor T31. *Id.* at 6:31–33. Capacitor C31 stores the data signal that is applied to the gate of transistor T31. *Id.* at 6:33–34. Each pixel includes transistor T34 for initializing the data signal stored in capacitor C31 in response to a previous scan signal SCAN[n-1], which was applied to a scan line just before the associated scan line. *Id.* at 7:3–6. Transistor T35 provides power supply voltage VDD for driving transistor T31 in response to current light-emitting signal. *Id.* at 52–55. Transistor T36 provides a driving current, generated through transistor T31, for EL element EL31 in response to current light-emitting signal. *Id.* at 6:55–58.

The '599 patent describes three different operations for the pixel circuit of Figure 3: an initialization operation, a data program operation, and a light-emitting operation. Ex. 1001, 7:15–64. The initialization operation initializes the data signal stored in capacitor C31, which provides the gate voltage of driving transistor 31. *Id.* at 7:24–26. The '599 patent explains:

> First, in an initialization operation, during an initialization period in which previous scan signal SCAN[n-1] is of a low level, and current scan signal SCAN[n] and light-emitting signal EMI[n] are of high level as shown in FIG. 4, since transistor T34 is turned on by the low level of previous scan signal SCAN[n-1], and transistors T31-T33 and T35-T36 are turned off by the high level of current scan signal SCAN[n] and current light-emitting signal EMI[n], an initialization path (as indicated by a solid line shown in FIG. 5) is formed. Accordingly, the data signal that has been stored in capacitor C31, namely, a gate voltage of driving transistor T31, is initialized.

Id. at 7:15–26 (bracketed material in original). Figure 5 of the '599 patent is reproduced below:

FIG. 5

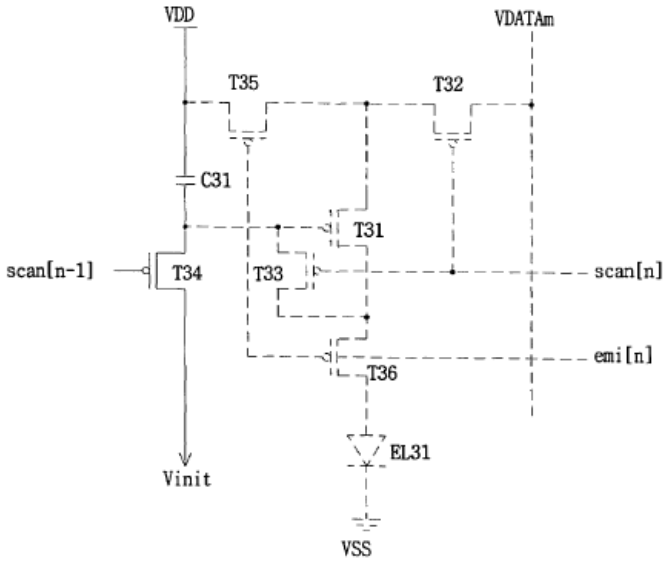


Figure 5 is a diagram for explaining the initialization operation of an embodiment of the pixel circuit of the '599 patent. *Id*. at 6:4–7.

The data programming operation applies a data voltage VDATAm to the gate of driving transistor T31 through threshold voltage compensation transistor T33. *Id*. at 6:41–44. The '599 patent explains:

> Next, in a data program operation, during a programming period in which previous scan signal scan [n-1] is at a high level, current scan signal SCAN[n] is at a low level and current light-emitting signal EMI[n] is at a high level as shown in FIG. 4, transistor T34 is turned off, and transistor T33 is turned on by the low level of current scan signal SCAN[n], such that driving transistor T31 is connected in the form of a diode.
>
> Since switching transistor T32 is also turned on by current scan signal SCAN[n], and switching transistors T35 and T36 are turned off by current light-emitting signal EMI[n], such that a data program path (as indicated by a solid line shown in FIG. 6) is formed. Accordingly, data voltage VDATAm applied to the associated data line is provided for the gate of driving transistor T31 through threshold voltage compensation transistor T33.
>
> Since driving transistor T31 is in the diode connection, VDATAm-$V_{TH(T31)}$ is applied to the gate of transistor T31 and the gate voltage is stored in capacitor C31, such that the program operation is completed.

Id. at 7:28–48 (bracketed material in original). Figure 6 of the '599 patent is reproduced below:

FIG. 6

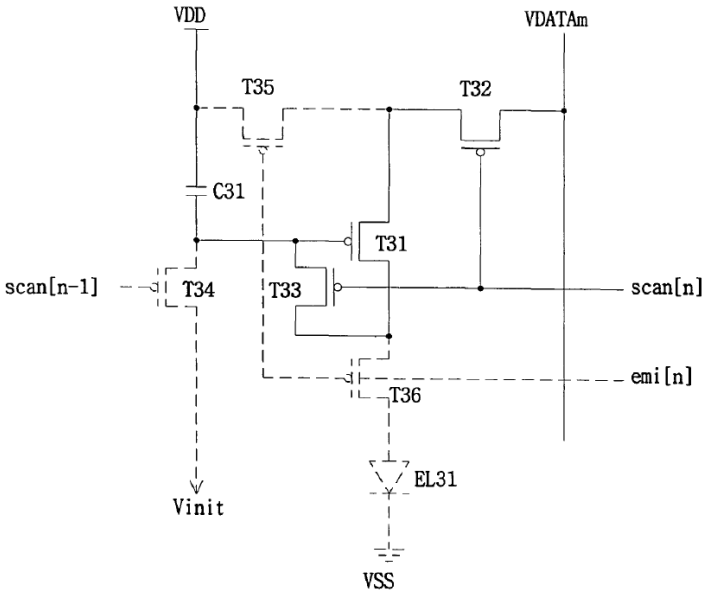


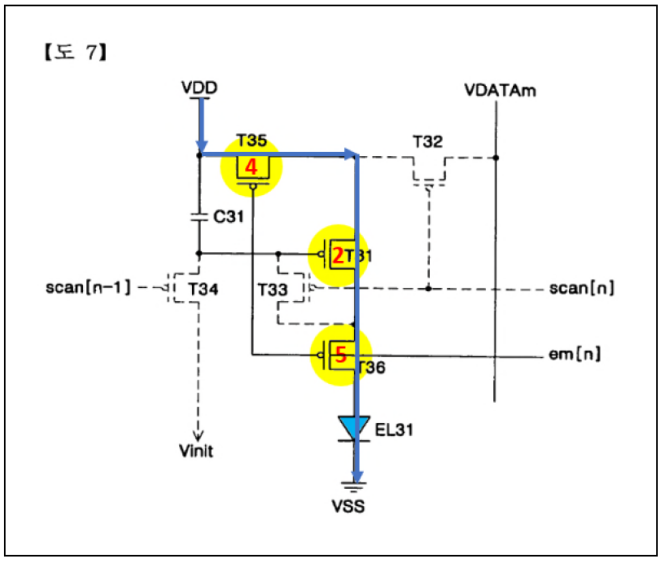
Figure 6 is a diagram for explaining the data program operation of an embodiment of the pixel circuit of the '599 patent. *Id*. at 6:4–7.

The light-emitting operation causes emission of light from light-emitting element EL31 by a driving current generated through transistor T31 in response to the data signal voltage applied to the gate of driving transistor T31. *Id*. at 7:60–64. The '599 patent explains:

> Finally, in a light-emitting operation, during an light-emitting period in which previous scan signal SCAN[n-1] is of high level, current signal SCAN[n] becomes a high level, and then current light-emitting signal EMI[n] becomes a low level as shown in FIG. 4, an light-emitting path (as indicated by the solid line as shown in FIG. 7) is formed. That is, switching transistors T35 and T36 are turned on by the low level of current light-emitting signal EMI[n], initialization transistor T34 is turned off by the high level of previous scan signal SCAN[n-1], and threshold voltage compensation transistor T33 and switching transistor T32 are turned off by the high level of current scan signal SCAN[n]. Accordingly, a driving current generated in response to the data signal voltage applied to the gate of driving transistor T31 is provided through transistor T31 for organic EL element EL31, such that the light-emitting of organic EL element EL31 occurs.

Id. at 7:49–65 (bracketed material in original). Although this description references a solid line indicating a light-emitting path in Figure 7, the drawing figure labeled "Figure 7" in the '599 patent does not have such a solid line. In fact, Figure 7 appears to mistakenly duplicate Figure 6 of the '599 patent. In the Petition, Petitioner refers instead to Figure 7 of the Korean patent application to which the '599 patent claims priority in order to illustrate the textual description in the '599 patent for Figure 7. Pet. 6 n.1; *see also* Ex. 1001, code (30) (foreign priority data); Ex. 1003 ¶ 101 (Dr. Foty reproducing the Korean application version of Figure 7). Patent

Owner does not dispute that there is inaccuracy in that regard. We accept Figure 7 of the Korean priority application of the '599 patent as Petitioner's illustration of the textual description in the '599 patent for Figure 7. We find that it is consistent with and also a reasonable depiction of the textual description in the '599 patent for Figure 7. Figure 7 of the Korean priority application of the '599 patent (as annotated by Petitioner) is reproduced below:



This figure is used by Petitioner to illustrate the textual description in the '599 patent for the light-emitting operation of the pixel circuit. Pet. 10–11.

Claims 1, 7, 14, 15, and 17 are independent. Claim 7 and 14 are representative and reproduced below:[2]

> [Claim 7 Preamble] A pixel circuit in an organic light emitting device, comprising:

[2] The bracketed labels correspond to those used by Petitioner to reference the claim elements. *See* Pet. 23–49, 67–70. We use the same labels here for ease of reference, understanding, and consistency.

[7a] a first transistor for delivering a data signal voltage in response to a current scan line signal;

[7b] a second transistor for programming the data signal voltage and for generating a driving current in response to a programmed data signal when light is emitted;

[7c] a third transistor for providing the data signal voltage for the second transistor in response to the current scan signal;

[7d] a capacitor for maintaining the data signal voltage programmed onto the second transistor;

[7e] a fourth transistor for delivering a power supply voltage to the second transistor when the light is emitted;

[7f] a fifth transistor for delivering the driving current, provided from the second transistor, in response to the data signal voltage when the light is emitted; and

[7g] an electroluminescent element for emitting light corresponding to the driving current delivered through the fifth transistor,

[7h] wherein the third transistor connects the second transistor in the form of a diode in response to the current scan signal so that the second transistor detects and compensates its threshold voltage deviation in itself.

Ex. 1001, 9:35–58.

[Claim 14 Preamble] A pixel circuit in an organic light emitting device, comprising:

[14a] an electroluminescent element for emitting light in response to an applied driving current;

[14b] a first transistor for delivering a data signal voltage in response to a current scan line signal;

[14c] a second transistor for generating a driving current to drive the electroluminescent element in response to the data signal voltage;

[14d] a third transistor for connecting the second transistor in the form of a diode in response to the current scan signal to self-compensate a threshold voltage of the second transistor;

[14e] a capacitor for storing the data signal voltage delivered to the second transistor;

[14f] a fourth transistor for delivering a power supply voltage to the second transistor in response to a current light-emitting signal; and

[14g] a fifth transistor for providing the driving current, provided from the second transistor, for the electroluminescent element in response to the current light-emitting signal.

Id. at 10:29–49.

E. Reference relied on by Petitioner and Declarations

Petitioner relies on the following reference:

"Kimura" -- U.S. Pub. Pat. App. 2003/0132931 A1, published July 17, 2003, based on Application No. 10/283,330, filed Oct. 30, 2002, and claims priority to JP 2002-298062, filed Oct. 10, 2002, and JP 2001-333575, filed Oct. 30, 2001. Ex. 1002, codes (21), (22), (30), (43).

Petitioner relies on the Declaration of Daniel Foty, Ph.D. (Ex. 1002) submitted with the Petition, and a Supplemental Declaration of Dr. Foty (Ex. 1029) submitted with Petitioner's Reply.

Patent Owner relies on the Declaration of Andrew Wolfe, Ph.D. (Ex. 2008 (filed in confidential and public version)), the Declaration of Aris Silzars, Ph.D. (Ex. 2043), and the Declaration of Kwangsae Lee (Ex. 2046 (filed in confidential and public version)), all submitted with the Patent Owner Response.

In support of its Opposition to Patent Owner's Motion to Exclude Evidence, Petitioner relies on the Declaration of Thomas L. Credelle, Ph.D. (Ex. 1035) which was provided by Petitioner as supplemental evidence. Paper 60, 3.

In support of its Opposition to Petitioner's Motion to Exclude Evidence, Patent Owner relies on a Supplemental Declaration of Dr. Wolfe. (Ex. 2055) which was filed by Patent Owner as supplemental evidence. Paper 61, 14.

F. Asserted Ground of Unpatentability

Petitioner asserts that the challenged claims of the '599 patent are unpatentable based on the following ground:

Claims Challenged	35 U.S.C. §[3]	Reference(s)/Basis
1–18	103	Kimura

Pet. 2.[4]

[3] The Leahy-Smith America Invents Act, Pub. L. No. 112–29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. §§ 102 and 103. Based on the record before us, we determine that the '599 patent has an effective filing date prior to the effective date of the applicable AIA amendments (March 16, 2013). We, therefore, refer to the pre-AIA version of 35 U.S.C. § 103.

[4] Petitioner actually states the ground of unpatentability as "over Kimura (EX1002) and Knowledge of POSITA [person of ordinary skill in the art]." Pet. 2. However, it is not necessary to expressly state "knowledge of a POSITA, because the obviousness determination is made form the perspective of "a person having ordinary skill in the art." 35 U.S.C. § 103.

II. ANALYSIS

A. Burden of Proof

The Petitioner has the burden of proving unpatentability by a preponderance of the evidence. 35 U.S.C. § 316(e). That burden never shifts to Patent Owner except in limited circumstances not present here. *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1375 (Fed. Cir. 2016). "Preponderance of the evidence means the greater weight of evidence, evidence which is, more convincing than the evidence which is offered in opposition to it." *United States v. C.H. Robinson Co.*, 760 F.3d 1376, 1383 (Fed. Cir. 2014) (internal quotations omitted).

B. Level of Ordinary Skill in the Art

Petitioner asserts the following with respect to the level of ordinary skill in the art:

> A person of ordinary skill in the art ("POSITA") in the technology field of the '599 patent would have had a Bachelor's degree in electrical engineering or similar discipline, along with 2-3 years of circuit design/analysis experience. *See* EX1003, ¶31. Lack of work experience can be remedied by additional education, and vice versa. *Id*.

Pet. 13 (citing Ex. 1003 ¶ 31).

Patent Owner proposes that a person of ordinary skill in the art "would have had a relevant technical degree in Electrical Engineering, Computer Engineering, Material Science, Physics, or the like, and experience in active matrix display design and electroluminescence." PO Resp. 7 (citing Ex. 2008 ¶¶ 45–49).

We need not resolve the difference between Petitioner's and Patent Owner's articulation of the level of ordinary skill in the art because, adopting Petitioner's articulation, we still determine that Petitioner failed to

prove by a preponderance of the evidence that any of the challenged claims is unpatentable. For our analysis below, we apply Petitioner's articulation of the level of ordinary skill in the art.[5]

C. Claim Construction

We use the same claim construction standard that would be used to construe a claim in a civil action under 35 U.S.C. § 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.100(b) (2022). The claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc) is applicable.

Claim terms are generally given their ordinary and customary meaning as would be understood by one with ordinary skill in the art in the context of the specification, the prosecution history, other claims, and extrinsic evidence including expert and inventor testimony, dictionaries, and learned treatises, although extrinsic evidence is less significant than the intrinsic record. *Phillips*, 415 F.3d at 1312–17. Usually, the specification is dispositive, and it is the single best guide to the meaning of a disputed term. *Id.* at 1315.

The specification may reveal a special definition given to a claim term by the patentee, or the specification or prosecution history may reveal an intentional disclaimer or disavowal of claim scope by the inventor. *Id.* at 1316. If an inventor acts as his or her own lexicographer, the definition

[5] All of our findings and conclusions would still be the same, however, had we applied Patent Owner's articulation of the level of ordinary skill in the art.

must be set forth in the specification with reasonable clarity, deliberateness, and precision. *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1249 (Fed. Cir. 1998). The disavowal, if any, can be effectuated by language in the specification or the prosecution history. *Poly-Am., L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1136 (Fed. Cir. 2016).

Only those claim terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

Petitioner asserts that "no term requires construction for this proceeding." Pet. 14. Patent Owner asserts that "[f]or purposes of this proceeding, Patent Owner does not believe any specialized constructions are necessary." PO Resp. 7. We agree with the parties that it is not necessary to conduct express construction for any claim term.[6]

D. Alleged Obviousness of Claims 1–18 over Kimura

1. The Law on Obviousness

A claim is unpatentable under 35 U.S.C. § 103(a) "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

[6] We reach this conclusion after having considered the construction of certain claim terms in the '599 patent by the Administrative Law Judge in the related USITC Investigation No. 337-TA-1351 (Ex. 2005, 13–15, 37–48).

subject matter pertains." 35 U.S.C. § 103(a); *see KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations, including commercial success, long-felt but unsolved needs, failure of others, and unexpected results. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966).

2. Overview of Kimura

Kimura relates to an active matrix light emitting device including a semiconductor device having a thin film transistor ("TFT"). Ex. 1002 ¶ 1. Kimura describes numerous embodiments of a pixel including a light-emitting device, some with the pixel including "first to third transistors" (*id.* ¶¶ 123, 139), some with the pixel including "first to fourth transistors" (*id.* ¶¶ 40, 54, 68, 82, 95, 110), and some with the pixel including "first to fifth transistors" (*id.* ¶¶ 156, 174, 192, 209, 228, 246).

The Abstract of Kimura describes:

> Brightness irregularities that develop in a light emitting device due to [dispersion] among pixels in the threshold values of TFTs used for supplying electric current to light emitting devices become obstacles to improved image quality of the light emitting device. As an image signal input to a pixel from a source signal line, a desired electric potential is applied to a gate electrode of a TFT for supplying electric current to an EL device, through a TFT having its gate and drain connected to each other. A voltage equal to the TFT threshold values is produced between the source and the drain of the TFT 105. An electric potential in which the image signal is offset by the amount of the threshold value is therefore applied to the gate electrode of the TFT. Further, TFTs are disposed in close proximity to each other within the pixel, so

> that dispersions in the TFT characteristics do not easily develop. A desired drain current can thus be supplied to the EL device even if there is dispersion in the threshold values of the TFTs among pixels, because this is offset by the threshold value of the TFT.

Ex. 1002, code (57).

We focus on the embodiment illustrated in Kimura's Figures 33A through 33E, referred to as Embodiment 9 in Kimura (Ex. 1002 ¶ 652), because Petitioner relies on this embodiment. Petitioner has annotated Figure 33A as shown below (Pet. 22):

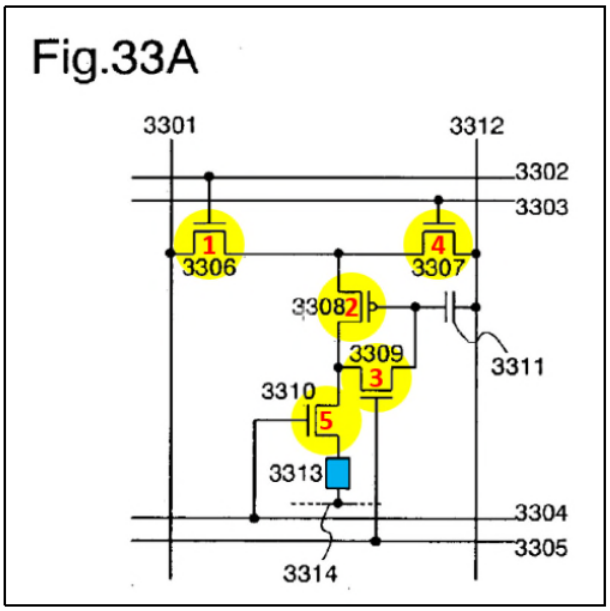
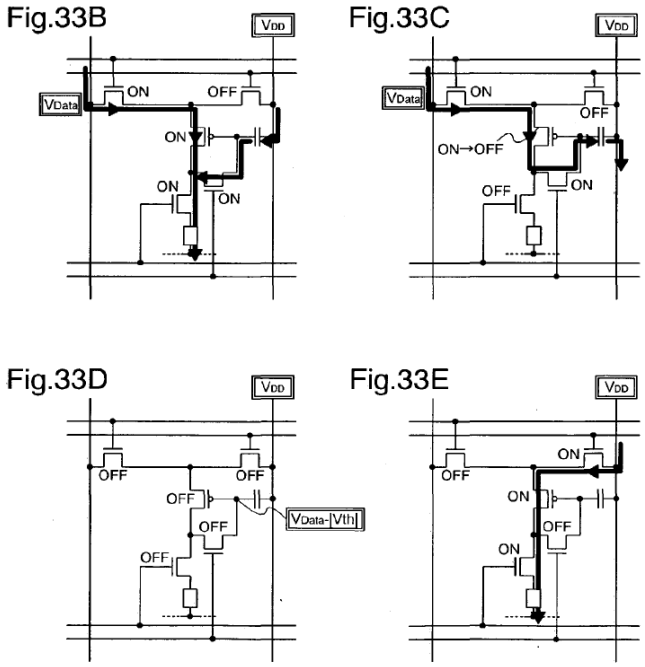


Figure 33A is one of several figures, 33A–33E, used to illustrate an embodiment of Kimura's device. Ex. 1002 ¶ 339. In this annotated version of Kimura's Figure 33A, Petitioner has highlighted in yellow transistors 3306, 3308, 3309, 3307, and 3310, and numbered them in red as "1," "2," "3," "4," and "5," respectively (hereinafter Transistors 1–5), and also highlighted in blue electroluminescent ("EL") device 3313. Hereinafter, we

use the same numbering when referring to these transistors in Figures 33B, 33C, 33D, and 33E.

Figures 33B–33E of Kimura are reproduced below:



Figures 33B–33E are the remainder of the figures used to illustrate the same 9th embodiment of Kimura's device. Ex. 1002 ¶ 339. They show the ON/OFF states of each transistor, and the current path in bold.

As shown above in Figure 33A, TFT 3309 (Transistor 3) is connected between the gate electrode and the drain electrode of TFT 3308 (Transistor 2), and Transistor 2 exhibits the behavior of a diode connected TFT when Transistor 3 is on. *Id.* ¶ 654. Kimura explains:

> Operation is explained. First, the TFT 3306 turns on, and an image signal VData is input as shown in FIG. 33B. In addition, The TFT 3309 and a TFT 3310 turn on, and the *TFT 3308 thus behaves as a diode connected TFT*. When the TFT 3310 then turns off electric charge moves as shown in FIG. 33C. The voltage between the source and the drain of the TFT 3308, in other words the voltage between the gate and the source of the

> TFT 3308, eventually becomes equal to the threshold voltage, at which point the TFT 3308 turns off as shown in FIG. 33D.
>
> The TFTs 3307 and 3310 then turn on. The electric potential of a source region of the TFT 3308 increase from VData to VDD as the TFT 3307 turns on. The voltage between the gate and the source of the TFT 3308 therefore exceeds the threshold voltage to cause it to turn on, so that electric current flows in the EL device 3313 to cause it to emit light, as shown in FIG. 33E.
>
> Thus, an electric potential difference equal to the threshold value can be produced between the gate and the source of the driver TFT 3308 in advance in accordance with the above processes, so that even if there is dispersion in the threshold voltages of the TFTs 3308 between adjacent pixels, there is no dispersion in the voltages between the gate and the source of the driver TFTs 3308 of adjacent pixels. In addition, *correction of dispersions in the threshold values is performed in the foregoing embodiments by a method in which the threshold voltage of a diode connected TFT is added to the image signal*, and then input to the gate electrode of another driver TFT.

Id. ¶¶ 655–657 (emphasis added).

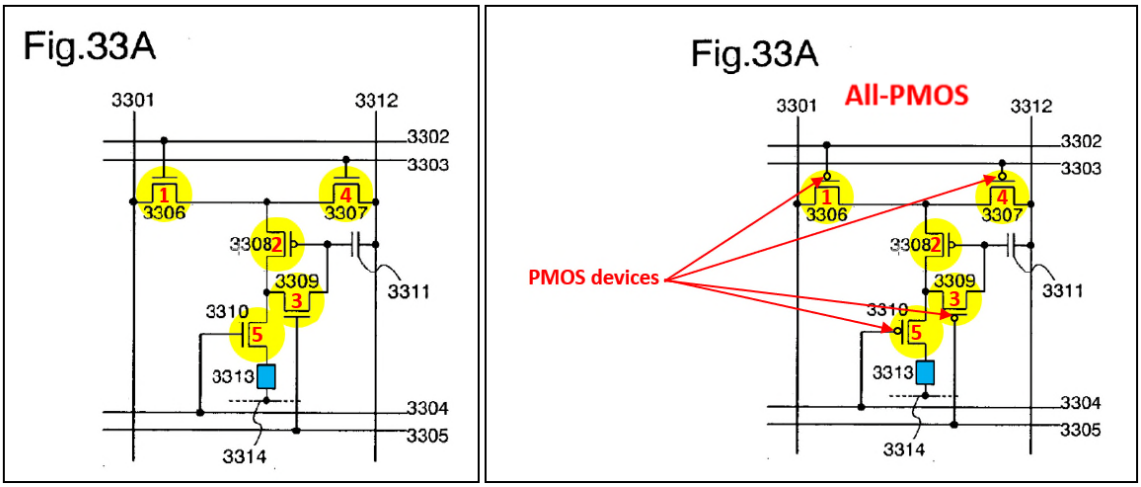
3. Overview of the Technical Issues

Three technical matters are at issue: (1) Petitioner's assertion that it would have been obvious to one of ordinary skill in the art to modify Kimura's Figure 33 embodiment to use only pMOS transistors (hereinafter "All pMOS Transistors Issue"); (2) Petitioner's accounting for a feature that requires shared control of 4th and 5th transistors in claim 13 which depends from claim 7 and in independent claims 14, 15, and 17, and 5th and 6th transistors in independent claim 1 (hereinafter "Shared Control of Two Transistors Issue"); and (3) Petitioner's accounting for a feature regarding an additional initialization transistor in dependent claims 2, 8, 16, and 18 (hereinafter "Initialization Transistor Issue"). As discussed below, Petitioner has not persuasively shown that a POSITA would have modified

Kimura's Figure 33 embodiment to use only pMOS transistors, which is dispositive as to all challenged claims. Petitioner also has not persuasively shown that a POSITA would have modified Kimura's Figure 33 embodiment to have two transistors driven by a shared input signal as the resulting circuit does not work or is inoperative for the pixel circuit, which is further dispositive as to claims 1–6 and 13–18. We do not reach the Initialization Transistor Issue.

4. *The All pMOS Transistors Issue*

Petitioner states: "Before the element-by-element patentability analysis, it is helpful to discuss a modification to Kimura Fig. 33 [Figs. 33A-33E]." Pet. 19. That is a modification which replaces all nMOS transistors with pMOS transistors such that the only transistors used in the embodiment shown Figures 33A–33E are pMOS transistors. Pet. 19–23. The modification is shown on page 22 of the Petition via a side-by-side illustration of the before and after views of the modification to Figure 33A, with colored annotations added by Petitioner, as reproduced below:



ORIGINAL MODIFIED

In the version of Figure 33A on the left, labeled "ORIGINAL," Petitioner numbered in red Transistors 1–5 and colored them yellow, as well as colored EL element 3313 blue. In the modified version of Figure 33A on the right, labeled "MODIFIED," Petitioner changed the symbols for Transistors 1, 3, 4, and 5 from nMOS to pMOS, and pointed to them as "PMOS devices" with red arrows. Transistor 2 in the original version is pMOS and remains unchanged by the modification.

Petitioner uses the modified Figures 33A–33E (nMOS transistors 1, 3, 4, and 5 all changed to pMOS transistors so that all transistors are pMOS) to support its assertions of unpatentability of all challenged claims including each independent claim. *See, e.g.*, Pet. 24–49, 72–73, 76–78, 81, 86–93. Petitioner explicitly states immediately after the two side-by-side figures reproduced above: "*Petitioner uses the modified 'ALL-PMOS" version of Fig. 33 for the patentability analysis and includes the label 'All-PMOS' for clarity.*" *Id.* at 22 (emphasis added).

None of the independent claims includes an express limitation with regard to whether all of the recited transistors therein must be pMOS. Petitioner, however, asserts that based on the connections recited within them, independent claims 15 and 17 each require all recited transistors therein to be pMOS transistors. Pet. 71–72, 80. Patent Owner expresses no disagreement. Even for independent claims 1, 7, and 14, Petitioner relies on its all pMOS modification of Kimura's Figure 33 embodiment. Pet. 22 ("Petitioner uses the modified 'All-PMOS' version of Fig. 33 for the

patentability analysis . . . .”). Thus, to prevail on any challenged claim,[7] Petitioner must show that one with ordinary skill in the art would have had reason or motivation to convert Kimura’s Figure 33 embodiment to an all pMOS transistors version of the same embodiment.

Petitioner acknowledges that all transistors in Kimura’s unmodified “Figure 33” are nMOS transistors except for the driving transistor, i.e., transistor 3308 identified as Transistor 2, which is pMOS.[8] Pet. 39. Petitioner asserts:

> Kimura repeatedly and expressly teaches the interchangeability of NMOS and PMOS transistors used as switches, which is the case for all but the second transistor. *See, e.g.*, EX1002, [0438] (“Note that a structure is used [in Figs. 3B-3D] in which the TFTs 304 and 306 are n-channel TFTs. . . . **However, the TFTs 304 and 306 function as simple switching devices, and therefore any polarity may be used**.”); *id.*, [0396] (same for Figs. 1-2); *id.*, [0445] (same for Figs. 4B-4D); *id.*, [0649] (“All other TFTs are only used as switching devices for performing only on and off control, and therefore may be of any polarity.”); *id.*, [0362] (showing an all-PMOS driver circuit in Fig. 22); EX1003, ¶¶146-154.

Id. at 19–20 (alteration in original). Petitioner also asserts that the “interchangeability of NMOS and PMOS *switching transistors* was well-known by 2003.” *Id*. at 4 (citing Ex. 1004, 12:30–49) (emphasis added). Petitioner’s expert, Dr. Foty, testifies:

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[7] Petitioner is the master architect of its own Petition. *See SAS Inst., Inc. v. Iancu*, 584 U.S. 357, 366, 138 S. Ct. 1348, 1356 (2018) (“[T]he petitioner’s petition, not the Director’s discretion, is supposed to guide the life of the litigation.”).

[8] We understand that when Petitioner refers to Figure 33 of Kimura, Petitioner is referring to Kimura’s Figures 33A–33E, because there is no “Figure 33” in Kimura. We adopt the same usage to maintain consistency.

> *If the design need is for a transistor to be used as a simple on/off switch, then either an nMOS transistor or a pMOS transistor can be chosen* – since, as shown in the figure from Kang and Leblebici 2003 above, each can function as a simple on-off switch. As the primary operational difference between nMOS and pMOS (when a simple switch is desired) is that the on/off characteristics are the opposite of each other – and the on-off signals to be applied must be altered (i.e., reversed as it were) to account for this. In particular, as described in Section VII.A.1, nMOS devices turn on in response to a "high" voltage on the gate terminal and turn off when a "low" voltage is applied. This is known in the art as "active-high" signaling. pMOS transistors are just the opposite – they turn on when a "low" voltage is applied to the gate terminal and turn off in response to a "high" voltage on the gate. This is known in the art as "active-low" signaling. *Changing the polarity of a switching transistor (from nMOS to pMOS or vice versa) would require changing the polarity of the gate signal to achieve the same functionality, but doing so was easy and well-known to a POSITA.* In contrast, swapping an nMOS transistor that performs an analog-like function for a pMOS transistor (or vice versa) may be more difficult, no such change is proposed in this IPR.

Id. ¶ 57 (emphasis added) (cited at Pet. 4). Dr. Foty further explains that "if only one [transistor] species (nMOS or pMOS) is used exclusively in a circuit, then the [manufacturing] process complexity and the cost [of manufacturing] will be lower." *Id.* ¶ 58 (cited at Pet. 4). Dr. Foty testifies that if the change is made in Kimura to use only pMOS transistors, that "would result in a single-transistor-species circuit which would be simpler and less costly to manufacture." *Id.* ¶ 151 (cited at Pet. 20).

Petitioner additionally cites U.S. Patent No. 6,362,798 (Ex. 1004, "Kimura '798")[9] as supporting Petitioner's assertion that "interchangeability of NMOS and PMOS switching transistors was well-known by 2003." Pet. 4 (citing Ex. 1004, 12:30–49). The cited portion of Kimura '798 states:

> Moreover, the example shown in FIG. 1 is constructed with the mixture of a P channel type TFT and an N channel type TFT, however, every TFT can be N channel type TFTs or all TFTs can be P channel type TFTs. However, in consideration that the voltage/current characteristics and threshold characteristics of the driving TFTs 110 are compensated by the compensating TFT 120, it is advantageous to construct these driving TFTs 110 and compensating TFTs 120 by the same process as the same type TFTs. Particularly, if both TFTs are formed in the same film forming process, the degree of characteristics similarities between both TFTs generally increases, so that it becomes possible to provide the transistor circuit 100 on the same substrate with little or no variance in voltage/current characteristics and threshold characteristics. On the other hand, the resetting TFT 130 and *the switching TFT 140 can be either a P channel type TFT or an N channel type TFT without being dependent on whether the driving TFT 110 is a P channel type TFT or N channel type TFT*. However, it is often advantageous in manufacturing when all TFTs are of the same type.

Ex. 1004, 12:30–49 (emphasis added).

Petitioner asserts that one of ordinary skill in the art "would have had far more than a reasonable likelihood of success as making such changes [to use all pMOS transistors] was common place and well within a POSITA's skill." Pet. 21–22 (citing Ex. 1003 ¶ 154).

[9] Kimura '798 was issued Mar. 26, 2002, from Application 09/424,043, based on PCT/JP99/01342, filed Mar. 17, 1999, and claims priority to JP 10-069147, filed Mar. 18, 1998. Ex. 1004, codes (21), (22), (30), (45), (86).

We have considered Petitioner's rationale for modifying the embodiment in Kimura's Figures 33A–33E. It is based on two theories: (1) a first theory based on general interchangeability of nMOS and pMOS transistors which are used as *switching transistors*, and (2) a second theory that a single-transistor-species circuit is simpler and less costly to manufacture. We discuss them in sequence, first the general interchangeability rationale, and then the manufacturing benefits rationale.

a) Interchangeability of nMOS and pMOS Transistors

According to Petitioner, some transistors are "switching transistors" and some are not, and for "switching transistors," nMOS and pMOS configurations are interchangeable. Pet. 4, 19–20. On that basis, Petitioner asserts that using either an nMOS transistor or a pMOS transistor as a switching transistor is "a simple and obvious design choice" for one of ordinary skill in the art. Pet. 21.

Although the designation of a transistor as a "switching transistor" is critical to Petitioner's theory of obviousness, the Petition fails to explain what makes Transistor 3 in Kimura's Figure 33 embodiment merely a "switching transistor." Petitioner does not persuasively show that Kimura's Transistor 3 is a "switching transistor" consistent with its rationale for modifying a transistor from nMOS to pMOS.

Alternatively, even if Transistor 3 in Kimura's Figure 33A were a switching transistor, Petitioner still has not sufficiently shown a reason to modify Transistor 3 from nMOS to pMOS. Patent Owner presents persuasive evidence that, based on the particular role of Transistor 3 in Kimura's Figure 33 embodiment, Petitioner's proposed modification of Transistor 3 from nMOS to pMOS would result in consequential leakage

current effects that have not been addressed by Petitioner. The evidence Patent Owner has presented undermines Petitioner's reliance on a general theory of interchangeability in modifying Transistor 3 from nMOS to pMOS.

Patent Owner asserts that "A POSITA would have understood there were material differences between NMOS transistors and PMOS transistors relevant to, and that would affect the design and operation of, a pixel circuit for an AMOLED display." PO Resp. 13 (citing Ex. 2008 ¶¶ 63–68).

Patent Owner explains:

> Kimura discloses pixel circuits comprised of polysilicon thin-film transistors. *See, e.g.*, Kimura at ¶357; Ex. 2008, ¶63. In polysilicon TFTs, it was known that NMOS transistors were less susceptible to leakage current relative to PMOS transistors. Ex. 2008, ¶63; *see, e.g.*, Ex. 2049, Study of Leakage Current in n-channel and p-channel Polycrystalline Silicon Thin-Film Transistors by Conduction and Low Frequency Noise Measurements, C.T. Angelis, et al., J. Appl. Phys. 82, 4095–4101 (1997) ("The substantially lower leakage current observed in the n-channel polysilicon TFT is explained by the development of positive fixed charges at the interfaces near the drain junction which suppress the electric field."); E. 2050 (Foty Tr.) at 98:14–20. NMOS TFTs were further known to have higher mobility, and therefore to be faster, than PMOS TFTs. Ex. 2008, ¶64; Ex. 2050 at 92:20–93:20 (acknowledging a roughly 2:1 higher electron mobility in NMOS transistors). And at this time a POSITA would have understood that NMOS TFTs had the advantage of being smaller than comparable PMOS TFTs. Ex. 2008, ¶65; Ex. 2050 at 93:21–94:18.

PO Resp. 13–14.

Patent Owner further explains:

> For example, the difference in leakage current may present significant operational issues if transistor 3309 in Figure 33 [Transistor 3 as referred to by Petitioner] were modified to be PMOS (i.e., the transistor in Kimura that Petitioner claims

> corresponds to the "third" transistor of the '599 Patent). As Dr. Wolfe explains, *the "third" transistor controls charge flow to the capacitor and holds the programmed data for the pixel to maintain the intended brightness level*. Ex. 2008, ¶70. Kimura discloses that this transistor is NMOS. Kimura Fig. 33A. Nowhere does Kimura suggest that this transistor (or a transistor arranged in this way) may be modified from NMOS to PMOS. Ex. 2008, ¶70. On the contrary, the potential for greater leakage current in the PMOS transistor would be particularly significant for this "third" transistor, as any leakage could alter the stored brightness level, where Kimura was attempting to secure emission at an intended brightness level. *Id.*
>
> In addition, the faster speed of NMOS transistors would need to be taken into account with respect to the circuit's timing. Their difference in size would also influence the overall size (i.e., area) of the circuit, an important issue in display design. As Dr. Foty acknowledged, a reduction in circuit area allows for a larger aperture ratio. Ex. 2050 at 39:6–18; Ex. 2008, ¶65. A POSITA would have had no motivation to make unnecessary circuit modifications that would increase the circuit area, thus lowering the display's aperture ratio.

Id. at 14–15 (emphasis added).

In its Reply, Petitioner responds to Patent Owner's assertion regarding leakage by stating:

> Concerning leakage, Samsung asserts that replacing Kimura's "third transistor" (3309) with a PMOS transistor was nonobvious because it "could alter the stored brightness level" during light emission due to higher PMOS leakage. POR, 14. First, neither the '599 patent (EX1001, EX1028, 174:8-10) nor Kimura (Ex1002) say anything about leakage, reflecting it wasn't a meaningful concern. Second, Dr. Wolfe admitted that leakage does "not necessarily" affect pixel brightness "in a perceptible manner." EX1028, 173:21-174:3. Moreover, Samsung omits that the capacitor is intentionally discharged and then recharged **every cycle** during initialization and programming. *See* Kimura, Figs. 33B/36B, 33C/36C, [0655];

> EX1001, Figs. 5-6, 7:15-48; EX1028, 176:2-178:18. Thus, the capacitor need not hold charge for an extended time, making modest leakage unimportant. EX1029, ¶¶44-54.

Reply 6–7.

Petitioner's reply misses the point made by Patent Owner. It is not Patent Owner's burden to show nonobviousness. Nor has Patent Owner presented a nonobviousness argument. Rather, Patent Owner is noting technical and material differences between nMOS and pMOS transistors, in the context and application of a pixel circuit for an OLED, that undermine Petitioner's rationale for applying the general principle of interchangeability between an nMOS transistor and pMOS transistor.

Petitioner does not dispute that a pMOS transistor would have additional leakage current compared to an nMOS transistor. Nor does Petitioner dispute that this excess leakage current may affect pixel brightness and thus the operation of a pixel circuit for an AMOLED display. Petitioner characterizes this fact as "unimportant." Reply 7. We agree with Patent Owner that "leakage was a relevant consideration that needed to be assessed (and controlled) to avoid operational problems." Sur-reply 16. Dr. Wolfe explains that "[t]he idea is to design something so that the impact of the leakage is imperceptible." Ex. 1028, 174:2–3. We credit that testimony and are persuaded thereby.

Equally misplaced and unpersuasive is Petitioner's argument that neither the '599 patent itself nor Kimura "say anything about leakage, reflecting it wasn't a meaningful concern." Reply 7. Patent Owner correctly notes:

> While Kimura may not identify leakage current concerns in its actual embodiments, at issue are Petitioner's proposed

> modifications to Kimura's embodiments, modifications Kimura does not discuss nor contemplate. Significantly, Kimura identifies the particular transistors that could be either NMOS or PMOS, and it never states the transistor in Figure 33 that Petitioner maps to the claimed "third" transistor could be a PMOS transistor.

Sur-reply 16. Additionally, that the '599 patent itself does not discuss leakage current issues with respect to pMOS transistors does not mean there are none. At most it could just mean the leakage does not render the pMOS transistor unusable in a pixel circuit. The silence does not render nMOS and pMOS transistors technical equivalents for all roles within a pixel circuit.

Petitioner also notes that the '599 patent itself identifies no benefits or drawbacks of pMOS versus nMOS transistors and even states: "the pixel circuit can be configured of a NMOS transistor, a CMOS transistor or the like other than the PMOS transistor." Reply 4 (quoting Ex. 1001, 8:36–38). According to Petitioner, "[t]his passing statement reflects that a POSITA would have known about PMOS/NMOS interchangeability; otherwise the claims lack enablement and/or written description." *Id.* at 4–5.

Petitioner's argument is misplaced and unpersuasive. The cited statement does not refer to any particular transistor within the pixel circuit. Moreover, the Petition neither references the cited statement nor discusses how an ordinarily skilled artisan would have applied the same to the transistors in Kimura's pixel circuit. Further, if we were to assume that the cited statement refers to a non-switching transistor, then it does not aid Petitioner's theory of interchangeability for switching transistors. If we were to assume that the cited statement refers to a switching transistor, it is also of little help to Petitioner who, as discussed above, has failed to

establish that Transistor 3 in Kimura's Figure 33 embodiment is a switching transistor.

Also, the referenced statement is a description of additional embodiments of the '599 patent, i.e., the invention of the '599 patent, and not a description or acknowledgement of what would have been known to one of ordinary skill in the art. Further, it is not an admission by the inventors of the '599 patent that changing a transistor from one configuration to another would have no consequences and would be free of performance considerations. We also disagree that the '599 patent would lack enabling disclosure or written description support unless all transistors are deemed to be interchangeable between nMOS and pMOS configurations. Petitioner does not cite any supporting authority for that proposition. Nor does Petitioner provide meaningful reasoning. Accordingly, we do not agree that the issues of enabling disclosure and adequate written description are necessarily tied to the alleged interchangeability of nMOS and pMOS transistors in the manner suggested by Petitioner.

For these reasons, the vague statement in the Specification of the '599 patent does not sufficiently aid Petitioner in proving that one of ordinary skill in the art would have wanted to change transistor T3 in Kimura's Figure 33 embodiment from nMOS to pMOS.

We need not analyze other alleged differences between an nMOS transistor and a pMOS transistor in the context of a pixel circuit, e.g., alleged faster speed and smaller size of nMOS transistors,[10] because the leakage

[10] Petitioner asserts that "PMOS transistors could be the same size as NMOS transistors without perceptibly impacting refresh rate." Reply 6 n.5.

current issue alone raises sufficient doubt about Petitioner's rationale. Even if one could still have an operational pixel circuit by forming transistor 3309 with a pMOS transistor rather than an nMOS transistor, the larger leakage current of a pMOS transistor, in that context, still imparts a meaningful difference between the two configurations. The record is devoid of evidence showing countervailing benefits from making this change. We find that the potential disadvantage of added leakage current undermines Petitioner's alleged general principle of interchangeability between nMOS and pMOS transistors.

For the foregoing reasons, we determine that Petitioner has not persuasively shown that Kimura would have suggested to one of ordinary skill in the art that Kimura's Transistor 3 could be changed from nMOS to pMOS based on an alleged general interchangeability principle for "switching transistors."

b) Alleged Manufacturing Benefits for Forming All Transistors from a Single Species of Transistors

In the Decision on Institution, we questioned the completeness of Petitioner's second theory for forming all transistors in Kimura's Figure 33 embodiment with pMOS transistors. Inst. Dec. 31. We stated:

> The second theory appears incomplete because what is shown in Figures 33A–33E is merely a pixel circuit and does not include other components which are fabricated on the same substrate. Patent Owner notes that in addition to the pixel circuit, Kimura discloses a CMOS driver circuit, separate from the pixel circuit, on the same semiconductor substrate, which includes complementary nMOS and pMOS transistors. [Prelim. Resp.] 36. Petitioner has not asserted, much less explained, the interchangeability of a CMOS pair of nMOS and pMOS transistors with either two nMOS transistors or two pMOS transistors.

> At this stage, the record does not show sufficiently how a circuit would stay operative if a CMOS pair of nMOS and pMOS transistors were replaced with two nMOS transistors or two pMOS transistors. Petitioner does not explain how two nMOS transistors or two pMOS transistors would provide the same outputs, as seen from the other connected elements in the circuit, as a CMOS pair of complementary nMOS and pMOS transistors. The parties may further develop this issue subsequent to institution of trial. On the current record, we are not persuaded by Petitioner's second theory in support of an all p-MOS version of Kimura's Figure 33 embodiment.

Inst. Dec. 31–32.

Despite our inviting the parties to address our concern on Petitioner's second theory, Petitioner chose not to provide any further briefing. Petitioner's Reply does not include any further explanation or clarification. Thus, we continue to have the same concerns and the same doubts with respect to Petitioner's second theory for converting all nMOS transistors in Kimura's Figure 33 embodiment to pMOS transistors on the basis that it would have manufacturing benefits for using transistors of a single species, e.g., nMOS or pMOS, for all of the transistors in the Figure 33 embodiment.

In its Response, Patent Owner essentially reiterates its arguments from the Preliminary Response, asserting:

> Thus, even assuming there could be any "advantage[] in manufacturing when all TFTs are of the same type" in designs like those of the unrelated reference of Exhibit 1004 (Ex. 1004 at 12:30–49), any such advantage would not apply to Kimura's Figure 33. Ex. 2008, ¶77. Kimura's active matrix substrates include both NMOS and PMOS transistors in the driver portion, and thus even an all-PMOS redesign of Figure 33 (which is solely the pixel portion of the substrate) would not result in a substrate containing "all TFTs . . . of the same type" (Ex. 1004 at 12:30–49).

PO Resp. 25. Patent Owner further notes that while Petitioner cites to Kimura '798 (Ex. 1004) for its mentioning of "advantageousness in manufacturing" transistors of the same type, the advantages are for the circuits of Kimura '798, not for all circuits. *Id.* at 24. Patent Owner additionally asserts:

> As the Board observed in its institution decision, the single paragraph in the Petition relating to purported manufacturing benefits stemming from using a single species of transistor is "incomplete," and "Petitioner has not asserted, much less explained, the interchangeability of a CMOS pair of nMOS and pMOS transistors with either two nMOS transistors or two pMOS transistors." ID at 31.

PO Resp. 20.

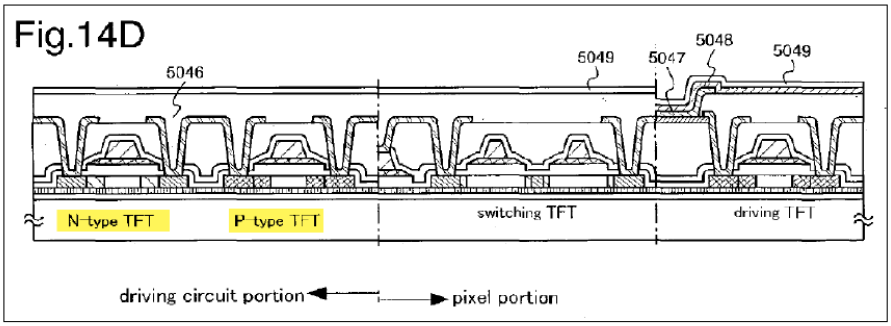
Patent Owner describes Kimura in additional detail, to explain how Kimura's active matrix devices include a separate circuit, apart from the pixel circuit shown in Figure 33, that includes CMOS pairs of nMOS and pMOS transistors:

> Petitioner's theory of an alleged manufacturing benefit to an all-PMOS circuit has no support. Indeed, it is inconsistent with Kimura's disclosures. Kimura is directed to active matrix devices formed using CMOS technology—i.e., circuitry that by its definition requires *both* PMOS and NMOS transistors. *See, e.g.*, Ex. 1011 at 5; Kimura at ¶¶547, 582. As Dr. Wolfe explains, a POSITA would not look to a reference teaching an improved CMOS process, like Kimura, only to abandon its CMOS design and teachings and implement a single-species modification. Ex. 2008, ¶ 76.
>
> Kimura includes extensive disclosures of using CMOS circuits, including detailed and specific manufacturing instructions to form pixel circuits and driver circuits that are both CMOS. Indeed, as noted above, Kimura expressly teaches that its process is directed to "*active matrix* light emitting device[s],"

Kimura at ¶1 (emphasis added), and Kimura explains that its "active matrix" devices necessarily includes CMOS circuitry:

> In this specification, a substrate in which [i] a driver circuit **including a CMOS circuit** and [ii] a pixel part having a switching TFT and a drive TFT are formed on the same substrate **is called an active matrix** substrate as a matter of convenience.

Kimura at ¶502 (emphasis added). Accordingly, Kimura teaches that its disclosed pixel circuits (the "pixel par")—including the embodiments relied upon by Petitioner—are used alongside CMOS driver circuits (e.g., for driving the signal line voltages), as part of the same substrate. Ex. 2008, ¶¶74–78. This can be seen in Figure 14D:



Kimura Fig. 14D (annotated)

PO Resp. 21–23. Figure 14D of Kimura is one of several diagrams illustrating a process of manufacturing a light emitting device according to Kimura. Ex. 1004 ¶320. Petitioner has highlighted the labels for the N-type TFT and the P-type TFT within the driving circuit portion.

Patent Owner further explains:

> Because the CMOS driver circuit and pixel circuits are formed together on the same active matrix substrate, the pixel circuits are (like the driver circuit) formed in a process that involves making both NMOS and PMOS transistors. Ex. 2008, ¶¶74–78. Indeed, Kimura includes detailed process steps for manufacturing its active matrix substrate consisting of both the driver circuit and pixel circuit, which results in the creation of both NMOS and PMOS TFT. Kimura at ¶¶502–615, Figs. 13–

> 15. Kimura explains that, by following its disclosed processing steps. "as shown in Fig. 14D, the driver circuit portion including the CMOS circuit composed of the N-channel TFT and the P-channel TFT and the pixel part including the switching TFT and the drive TFT can be formed on the same substrate." *Id.* at ¶547; *see id.* at ¶582. Even more, Kimura teaches that following its disclosed CMOS processing steps entails a manufacturing advantage—"the process is shortened and it can contribute to the reduction in manufacturing cost and the improvement of a yield." *Id.* at ¶571.

PO Resp. 23–24.

Patent Owner's assertions are rational and supported by the cited evidence. They are also unrebutted by Petitioner who chose not to address these issues in its Reply. We find that the substrate containing Kimura's pixel circuit also includes a driving circuit portion that includes both nMOS and pMOS transistors in a CMOS configuration. Accordingly, Petitioner's proposed all-PMOS redesign of Kimura's Figure 33 embodiment, which is only the pixel portion of the substrate, would not result in a substrate containing all transistors of the same type.

Thus, Petitioner does not persuade us that one of ordinary skill in the art would have changed all nMOS transistors in Kimura's Figure 33 to pMOS transistors to obtain manufacturing benefits of forming only transistors of a single type, i.e., pMOS. Additionally, Petitioner also has not balanced, from the perspective of one of ordinary skill in the art, the proposed modification of Figure 33 transistors to all be of a single type with Kimura's focus on and preference for having a CMOS design which includes both nMOS and pMOS transistors. *See Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006) (when "one motivating benefit

comes at the expense of another benefit, […] the benefits, both lost and gained, should be weighed against one another.").

5. Shared Control of Two Transistors Issue

We need not reach this issue, because on the All pMOS Transistors Issue discussed above in Section II.D.4, we already decided against Petitioner, and that is dispositive of all challenged claims 1–18.

However, although not necessary, we nonetheless still address the Shared Control of Two Transistors Issue, which is further dispositive of claims 1–6 and 13–18.

The issue is based on a limitation commonly recited in dependent claim 13, and independent claims 1, 14, 15, and 17. Petitioner specifically discusses the limitation in the context of dependent claim 13, and then, for the corresponding limitation in independent claims 1, 14, 15, and 17, refer back to its analysis for dependent claim 13. Pet. 64–65, 69–71, 74–75. We analyze claim 13 first as representative and then add further discussion for claims 1, 15, and 17.

Claim 13 depends from claim 7 and further recites:

> wherein the *fourth transistor* composed of a PMOS transistor including *a gate to which the current light-emitting signal is applied*, a source to which a power supply voltage is applied, and a drain coupled to the second transistor; and
>
> the *fifth transistor* is composed of a PMOS transistor including *a gate to which the current light-emitting signal is applied*, a source coupled to the second transistor, and a drain coupled to the electroluminescent element.

Ex. 1001, 10:20–28 (emphasis added). Petitioner acknowledges that claim 13 requires the gates of both the fourth and fifth transistors to be

controlled by "the current light emitting signal." Pet. 63. For that requirement, Petitioner relies on an "all-PMOS version of Kimura Fig. 36." *Id*. at 62–63. Petitioner explains:

> *Although Fig. 33B shows the fourth and fifth transistors controlled by different signals (viz., fourth transistor OFF while fifth transistor ON), that is not the case for Fig. 36.* EX1003, ¶257. *In all operation states of Fig. 36* (*viz*., Fig. 36B (initialization), Figs. 36C-D (programming), and Fig. 36E (light emission)), *the fourth and fifth transistors are always ON/OFF together*. EX1003, ¶257. *Thus a POSITA would have understood (or at least found it obvious) that Kimura uses a shared light-emitting signal to control them*. EX1003, ¶256-259. Kimura itself provides one reason for doing so—reducing the number of control lines improves aperture ratio. *See, e.g.*, EX1002, [0429]; *see also id*., [0421]-[0422] (control scheme with fewer signals reduces "surface area occupied by wirings in a pixel"). Additionally, the fourth and fifth transistors must both be active during light emission, otherwise the electroluminescent element will not emit light. EX1003, ¶¶138-140; *see also* EX1002, [0659] (signals "turn[ing] on and off at the same timing . . . can therefore be controlled by using the same gate signal line"). This, too, would have naturally led a POSITA to use a shared light-emitting signal. EX1003, ¶¶ 258-259.
>
> Moreover, Kimura discloses a timing diagram and control scheme utilizing only two signals (*i.e.*, first and second gate signals which map to the claimed "scan line signal" and "light emitting signal" respectively). *See* EX1002, Figs. 16-17 and explanation at [0420]-[0429]; EX1003, ¶259. This disclosure would have motivated a POSITA to use a shared light emitting signal for the fourth and fifth transistors and provided a reasonable expectation of success. EX1003, ¶259.

Id. at 64–65 (emphasis added).

In the Decision on Institution, we provided the following analysis:

> We agree that if the fourth and fifth transistors are always turned on and off together, as Petitioner asserts is the case for the

embodiment of Figures 36A–36E, there is reason for one of ordinary skill in the art to drive the fourth and fifth transistors by the same control signal, i.e., reducing the number of control lines and improving aperture ratio.

However, Petitioner's argument is questionable, because Petitioner's reasoning only has application to the embodiment of Figures 36A–36E, where the fourth and fifth transistors are always on and off together, and does not apply to the embodiment of Figures 33A–33E in which the fourth and fifth transistors do not always turn on and off together. If the fourth and fifth transistors in the Figure 33 embodiment were to be controlled by the same shared signal, such that they have to be turned on and off together, they would produce outputs and make current connections and disconnections inconsistent with what the other components in the pixel circuit of the Figure 33 embodiment expect from them. Petitioner does not explain the effect this inconsistency has on the operation of the Figure 33 embodiment, e.g., whether anything useful results from the change.

The Figure 36 embodiment is also different structurally from the Figure 33 embodiment in that it makes use of six transistors, not five as in the case of the Figure 33 embodiment. In accounting for claim 7, Petitioner relied on the Figure 33 embodiment to meet each of the limitations regarding the first, second, third, fourth, and fifth transistors. It is questionable whether the Figure 33 embodiment, after being modified to make the fourth and fifth transistor always turn on and off together, as Petitioner proposes based on the Figure 36 embodiment, would still meet all the requirements of the first, second, third, fourth, and fifth transistor, as recited in claim 7. Based on the present record, we find that Petitioner has not provided an adequate explanation as to this potential discrepancy.

Notably, we find the circumstance here to be different from Petitioner's proposal to modify all transistors of the nMOS type in Kimura's Figure 33 embodiment to pMOS type. In that proposal, the output of the switching transistor remains the same after the modification, and the other components in the pixel

> circuit, connected to the switching transistors, are unaffected by the modification. Here, the architecture differences between the embodiments in Kimura's Figures 33 and 36 result in different connections made and output signals provided to the other components in the pixel circuit. At this stage, Petitioner has not shown sufficiently that operations that used to be governed by a particular output from the fourth or fifth transistor in Figure 33 would continue to operate the same as they used to operate, when the output provided from the fourth or fifth transistor is different.
>
> For the foregoing reasons, we question Petitioner's reasoning presented to account for claim 13. The parties may further develop the issue subsequent to institution of trial.

Inst. Dec. 51–52 (footnote omitted).

In its Reply, Petitioner provided its response to the deficiency we noted above. Reply 9–18. However, for reasons discussed below, we are not persuaded by Petitioner's explanation. The same infirmities we articulated in the Decision on Institution, and as reproduced above, apply and undermine the Petition with respect to the Shared Control of Two Transistors Issue. The analysis from the Decision on Institution and reproduced above is adopted herein as a part of this Final Written Decision.

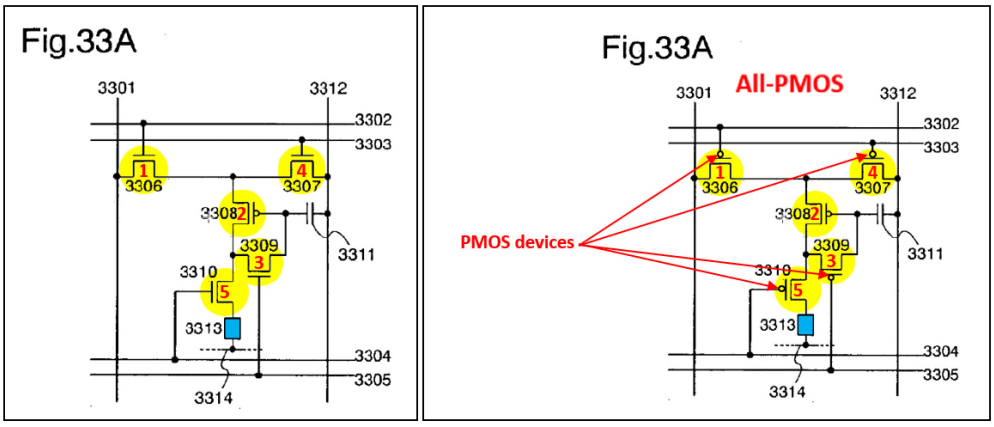
Petitioner does not dispute the reasoning we provided, as explained above, which leads to the conclusion that when modifying Kimura's Figure 33 embodiment to have transistors 4 and 5 driven by a shared input signal the resulting circuit does not work or is inoperative for the pixel circuit. Reply 10. Patent Owner's expert, Dr. Wolfe, has testified that the modification would result in an inoperable circuit. Ex. 2008 ¶ 97.

Petitioner appears to contend that the Petition already acknowledges that the modification would result in an inoperable circuity. Reply 10 (citing Pet. 64). We have again reviewed page 64 of the Petition and find that it

only conveys, as we previously understood, that the unmodified Figure 33 embodiment does not meet the required limitation. Fundamental to Petitioner's reply is Petitioner's assertion that it never proposed to change Kimura's Figure 33 embodiment. Reply 10. Petitioner asserts, rather, that it relied completely on Kimura's Figure 36 embodiment, to the exclusion of the Figure 33 embodiment, which does meet the requirement of controlling transistors 4 and 5 with a shared control signal. Reply 11. For numerous reasons, Petitioner's obviousness contentions necessarily rely on Kimura's Figure 33 embodiment, as explained below.

First, we revisit how the Petition begins its substantive analysis already discussed above in Section II.D.4.

Petitioner states: "Before the element-by-element patentability analysis, it is helpful to discuss a modification to Kimura Fig. 33 [Figs. 33A-33E]." Pet. 19. The modification is shown on page 22 of the Petition via a side-by-side illustration of the before and after views of the modification to Figure 33A, with colored annotations added by Petitioner, as reproduced below:



ORIGINAL MODIFIED

In the version of Figure 33A on the left, labeled "ORIGINAL," Petitioner numbered in red Transistors 1–5 and colored them yellow, as well as colored EL element 3313 blue. In the modified version of Figure 33A on the right, labeled "MODIFIED," Petitioner changed the symbols for Transistors 1, 3, 4, and 5 from nMOS to pMOS, and pointed to them as "PMOS devices" with red arrows. Petitioner explicitly states immediately after the two side-by-side figures reproduced above: "*Petitioner uses the modified 'ALL-PMOS" version of Fig. 33 for the patentability analysis and includes the label 'All-PMOS' for clarity.*" *Id.* at 22 (emphasis added).

Second, because claim 13 depends from independent claim 7 and thus incorporates all of the limitations from claim 7, we review how the Petition addresses claim 7. For limitation [7a], Petitioner relies on an all-PMOS version of Kimura's Figure 33C. Pet. 24–27. For limitation [7b], Petitioner relies on an all-pMOS version of Kimura's Figures 33C, 33D, and 33E. Pet. 30–32. For limitation [7c], Petitioner relies on an all-pMOS version of Kimura's Figures 33A and 34B. Pet. 32–36. For limitation [7d], Petitioner relies on an all-pMOS version of Kimura's Figures 33C and 33D. Pet. 37. For limitation [7e], Petitioner relies on an all-PMOS version of Kimura's Figures 33A and 33E. Pet. 39, 41. For limitation [7f], Petitioner relies on an all-PMOS version of Kimura's Figures 33A and 33E. Pet. 42–44. For limitation [7g], Petitioner relies on an all-PMOS version of Kimura's Figures 33A. Pet. 45. For limitation [7h], Petitioner relies on an all-PMOS version of Kimura's Figures 33A and 33D. Pet. 47–48.

As discussed above, Petitioner's analysis for claim 7 is tied exclusively to Kimura's Figure 33 embodiment. Further, Petitioner acknowledges that claim 13 depends from claim 7 (Pet. 62), and Petitioner's

obviousness contentions for claim 13 build upon and incorporate the claim 7 analysis. *Id.* at 62–67. Indeed, nothing in Petitioner's analysis for claim 13 indicates that Petitioner intended to depart from or otherwise modify its reliance on Figure 33 for teaching the limitations of the base claim. *See id.*

Petitioner identifies the following statement on pages 62–63 of the Petition: "the all-PMOS version of Kimura Fig. 36, discussed below, renders claim 13 obvious." Reply 11 & n.9 (quoting Pet. 62–63). However, by that statement Petitioner seems to rely on Figure 36 only for teaching the added limitations of claim 13, and Petitioner never states how such teachings would be reconciled with the Figure 33 teachings on which Petitioner relies for base claim 7. Also, in Petitioner's discussion of Kimura's Figure 36 embodiment with respect to claim 13, Petitioner does not revisit any of previously addressed limitations of claim 7 based on Kimura's Figure 33 embodiment.

In its Reply, Petitioner also notes that the Petition states that "Kimura Fig. 36 is merely an extension of Fig. 33 and discussion of one applies equally to the other unless noted." Pet. 15 n.3. The footnote appears in Section VI.A of the Petition which is titled "Description of Kimura," prior to and outside of the substantive analysis of any claim. It does not reasonably convey that Petitioner's substantive analysis for claim 13, as we explained above, is completely based on Kimura's Figure 36 embodiment and not at all on Kimura's Figure 33 embodiment.

Although Petitioner determines what it argues and thus is the master architect of its own Petition, *see SAS Inst.*, 584 U.S. at 366, Petitioner has a corresponding obligation and responsibility to make clear the positions it has taken and to not leave it to speculation and conjecture. It is too far a stretch,

and not a reasonable position to take, for Petitioner to assert that one should read its Petition as representing that for claim 13 Petitioner has jettisoned all reliance on Kimura's Figure 33 embodiment, and has based its analysis solely on Kimura's Figure 36 embodiment. Further, we note that Petitioner did not seek rehearing of our Decision on Institution, in which we expressed the same problem.

Third, Petitioner asserts that in our Decision on Institution, we invited Petitioner to develop the record on whether Kimura's Figure 36 embodiment would still meet all the requirements of the first, second, third, fourth, and fifth transistor in base claim 7. Reply 14 (citing Inst. Dec. 51–52). On that basis, Petitioner submitted additional testimony from its expert, Dr. Foty, Ex. 1029 ¶¶ 55–71, and discussed the same on pages 15 to 18 of the Reply. However, we did not make such an invitation.[11]

The Consolidated Trial Practice Guide (Nov. 2019) ("CTPG")[12] provides:

> Generally, a reply or sur-reply may only respond to arguments raised in the preceding brief. 37 C.F.R. § 42.23, except as noted above. "Respond," in the context of 37 C.F.R. § 42.23(b), does not mean proceed in a new direction with a new approach as compared to the positions taken in a prior filing. While replies and sur-replies can help crystalize issues for decision, a reply or sur-reply that raises a new issue or belatedly presents evidence

[11] We authorized the parties to further address whether "operations that used to be governed by a particular output from the fourth or fifth transistor in Figure 33 would continue to operate the same as when they used to operate, when the output provided from the fourth or fifth transistor is different." Inst. Dec. 52. We expected Petitioner to address how the Figure 33 embodiment would operate when and if modified to have the fourth and fifth transistors share the same control input.

[12] Available at https://www.uspto.gov/TrialPracticeGuideConsolidated.

> may not be considered. The Board is not required to attempt to sort proper from improper portions of the reply or sur-reply.

CTPG at 74.

To the extent that Petitioner's Reply purports to analyze claim 13 (and claim 7 from which it depends) based entirely on Kimura's Figure 36, we find that this represents a new direction with a new approach as compared to the positions Petitioner took in the Petition. *See id.* Accordingly, the submissions of Petitioner purportedly made in response to the Board's invitation, i.e., paragraphs 55–71 of Dr. Foty's reply Declaration (Exhibit 1029) and corresponding arguments discussed on pages 15–18 of the Reply, are not entitled to consideration and are not considered.

Fourth, another problem undermines Petitioner's assertion that it relied solely on Kimura's Figure 36 embodiment when accounting for claim 13 (and claim 7 from which it depends). The problem relates to Petitioner's analysis for claim 8 which, like claim 13, depends from claim 7. In that analysis for claim 8, Petitioner proposes adding an "initialization transistor" to Kimura's Figure 33 embodiment because the design of Figure 33 is susceptible to "undesired light emission." Pet. 51. Yet, as noted by Patent Owner, Kimura's Figure 36 embodiment already provides a solution to the undesirable light emission problem. Patent Owner explains:

> Petitioner's theory for adding an "initialization transistor" to Kimura Figure 33 notes that the design of Figure 33 "is less desirable" because of "undesired light emission." Pet. at 51. Kimura acknowledges this shortcoming in Paragraph 665:
>
> > In the structures shown FIGS. 33 to 35, there are cases in which ***electric current flows in the EL device to cause light emission***, before or after threshold voltage acquisition, that is ***during a period that is not the normal light emitting period***.

> . . . [T]his therefore causes errors to develop between the actual brightness and the target brightness.

Kimura at ¶665. However, Kimura provides its solution to this problem in the very next paragraph—namely, the circuit of Figure 36:

> ***A TFT 3612 is therefore added as shown in FIG. 36A*** . . . An electric current path to the L device 3615 is cut off by a TFT 3611, and therefore the EL device 3615 does not emit light. ***Light emission by the EL device during unnecessary periods can thus be prevented by using this type of structure***.

Kimura at ¶666 (emphasis added). Indeed, Petitioner elsewhere acknowledges that "Kimura solves this problem . . . as shown in Fig. 36B." Pet. at 19. Ex. 2008, ¶95.

PO Resp. 34–35. These assertions are supported by the cited evidence and not rebutted by Petitioner.

Petitioner's treatment of claim 8 reflects that Petitioner relied on Kimura's Figure 33 embodiment for all the limitations of independent claim 7, which also are incorporated into dependent claim 13.

Claim 14 is substantially the same as claim 7, except for limitations [14f] and [14g]. Claim 14 via limitation [14f] additionally requires the fourth transistor to deliver a power supply voltage to the second transistor "in response to a current light-emitting signal." Ex. 1001, 10:44–46. Claim 14 via limitation [14g] additionally requires the fifth transistor to provide drive current "in response to the current light-emitting signal." *Id.* at 10:47–49. These additional features of claim 14 are essentially the same as those required by claim 13, which recites that the fourth transistor includes "a gate to which the current light-emitting signal is applied," and that the fifth transistor includes "a gate to which the current light-emitting

signal is applied." *Id*. at 10:20–28. Like in the case of claim 7 from which claim 13 depends, Petitioner accounts for the other limitations of claim 14 by reliance on Kimura's Figure 33 embodiment. Pet. 67–69.

Claim 15 differs from claim 7 in its recitation of the fourth and fifth transistors. According to claim 15, the fourth transistor includes "a gate to which a current light-emitting signal is applied," and the fifth transistor also includes "a gate to which the current light-emitting signal is applied." Ex. 1001, 10:60–67. These additional features of claim 15 are the same as those required by claim 13, which recites that the fourth transistor includes "a gate to which the current light-emitting signal is applied," and that the fifth transistor includes "a gate to which the current light-emitting signal is applied." *Id*. at 10:20–28. Like in the case of claim 7 from which claim 13 depends, Petitioner accounts for the other limitations of claim 15 by reliance on Kimura's Figure 33 embodiment. Pet. 74–76.

Claim 17, like claim 15, recites that the fourth transistor includes "a gate to which a current light-emitting signal is applied," and that the fifth transistor includes "a gate to which the current light-emitting signal is applied." Ex. 1001, 12:4–11. These additional features of claim 17 are the same as those required by claim 13, which recites that the fourth transistor includes "a gate to which the current light-emitting signal is applied," and that the fifth transistor includes "a gate to which the current light-emitting signal is applied." *Id*. at 10:20–28. Like in the case of claim 7 from which claim 13 depends, Petitioner accounts for the other limitations of claim 17 by reliance on Kimura's Figure 33 embodiment. Pet. 83–86.

Claim 1 is similar to claim 7, but differs in several respects. Although, like claim 7, claim 1 recites five different transistors, claim 1

refers to them as first, second, third, *fifth, and sixth* transistors, rather than first, second, third, *fourth, and fifth* transistors as in claim 7. Petitioner refers to the skipping of the designator "fourth" as an "unusual numbering scheme," and as "an artifact from prosecution" where dependent claim 3 was rewritten into independent form. Pet. 11–12, 23. Specifically, application claim 1 had recited first, second, and third transistors, and application claim 3 depended from application claim 1 and further recited fifth and sixth transistors without reciting a fourth transistor. Ex. 1005, 415–416.

Because Petitioner regards the "fifth" and "sixth" identification of transistors simply as a numbering scheme without other significance, Petitioner performs its analysis as though "fifth" and "sixth" read the same as "fourth" and "fifth" in independent claim 7, and relies on the same reasoning as it presents for independent claim 7 to account for these differently named transistors of claim 1. Pet. 86–93. Patent Owner has not expressed disagreement with Petitioner's approach, and does not present arguments additional to those it presents for claim 7.

On this record, we accept that the designators "first," "second," "third," "fourth," "fifth," and "sixth" for the recited transistors in the claims merely identify particular transistors and do not, by themselves, set forth other requirements that need to be accounted for by Petitioner. *See 3M Innovative Properties Co. v. Avery Dennison Corporation*, 350 F.3d 1365, 1371 (Fed. Cir. 2003) (noting that the use of ordinals in a claim "is a common patent-law convention to distinguish between repeated instances of an element or limitation").

Claim 1 requires both the "fifth transistor" and "sixth transistor" to activate "in response to" the "current light-emitting signal." To account for

this requirement, Petitioner relies on the same reasoning it presents for essentially the same limitation in claim 13, that the fourth and fifth transistors each include "a gate to which the current light-emitting signal is applied." Pet. 91. Like in the case of claim 7 from which claim 13 depends, Petitioner accounts for the other limitations of claim 1 by reliance on Kimura's Figure 33 embodiment. *Id.* at 86–93.

Thus, the Shared Control of Two Transistors Issue is common to dependent claim 13 and independent claims 1, 14, 15, and 17. The deficiency discussed above for claim 13 equally applies to independent claims 1, 14, 15, and 17. This deficiency also applies to claims 2–6 which depend from claim 1, claim 16 which depends from claim 15, and claim 18 which depends from claim 17. Ex. 1001, 9:8–34, 11:8–13, 12:18–24.

Additionally, Petitioner's treatment of dependent claims 2, 16, and 18, which depend from claims 1, 15, and 17, respectively, further disproves that Petitioner intended to rely solely on Kimura's Figure 36 embodiment for claims 1, 15, and 17. Each of claims 16 and 18 requires an additional "sixth transistor" for performing initialization. Ex. 1001, 11:8–13, 12:18–24. Claim 2 requires an additional "fourth transistor"[13] for performing initialization. *Id.* at 9:8–12. Petitioner specifically discusses claim 8 and applies the same analysis to claims 2, 16, and 18. Pet. 49–56, 78–79, 86, 93.

Petitioner states: "[I]ncorporating the initialization transistor from Figs. 16-17 into Fig. 33 renders claim 8 obvious." Pet. 50–51. Petitioner again states: "Kimura Fig. 33 combined with the initialization transistor

[13] No "fourth transistor" is recited in claim 1 from which claim 2 depends. Ex. 1001, 8:53–9:7. Petitioner has treated the "fourth transistor" in claim 2 the same as it has treated the "sixth transistor" in claim 8. Pet. 93.

1607 from Fig. 16 renders claim 8 obvious." *Id.* at 56. These statements, as applied to claims 2, 16, and 18, contradict Petitioner's assertion that it relied solely on Kimura's Figure 36 embodiment to account for independent claims 1, 15, and 17.

Also, in accounting for the sixth transistor of claim 16 and 18 and the fourth transistor of claim 2, Petitioner's stated reason for adding the initialization transistor of Figures 16/17 to the Figure 33 embodiment is that the initialization performed in the Figure 33 embodiment is undesirably performed by the fifth transistor because "during initialization the current discharges through the light emitting element causing undesired light emission." Pet. 51. Petitioner further states:

> A POSITA would have been motivated to combine the initialization approach disclosed in Kimura Figs. 16-17 with Kimura Fig. 33 by adding a dedicated initialization transistor (*i.e.*, the sixth transistor as illustrated below). Ex.1003, ¶¶221-230 and ¶¶155-158. Such an approach is readily applicable to the baseline circuit of Fig. 33. *Id.*; *see also id.*, ¶¶141-143.

Id. at 52. These statements contradict Petitioner's assertion that it relied solely on Kimura's Figure 36 embodiment to account for independent claims 1, 15, and 17.

Had Petitioner actually based its analysis of the shared control limitations of the independent claims solely on Kimura's Figure 36 embodiment, then Kimura's ready-made solution to the light emission problem would nullify Petitioner's stated motivation in the context of dependent claims 2, 16, and 18, to look to Kimura's Figures 16/17 embodiment to add an initialization transistor.

6. Sixth Initialization Transistor Issue

This issue pertains only to dependent claims 2, 8, 16, and 18, which require a sixth initialization transistor and which depend from independent claims 1, 7, 15, and 17, respectively. Because we determine, as explained above in Section II.D.4, that Petitioner has not proved that Kimura would have suggested an all-pMOS version of Kimura's Figure 33 embodiment, which Petitioner relies on to account for all challenged claims 1–18, we need not reach the Sixth initialization Transistor Issue. We also have decided against Petitioner on the Shared Control of Two Transistors Issue, which is further dispositive of claims 1–6 and 13–18.

7. Secondary Considerations of Obviousness

We need not reach the issue of Patent Owner's objective evidence of nonobviousness because, for reasons discussed above, Petitioner's evidence of obviousness based on the teachings of Kimura does not support Petitioner's assertion that the challenged claims would have been obvious over Kimura. *See Magnavox Co. v. Activision Inc.*, 848 F.2d 1244, 1988 WL 44721 *1 (Fed. Cir. 1988) (unpublished). Even without considering Patent Owner's evidence of nonobviousness, we determine that Petitioner has not proved obviousness of any challenged claim by a preponderance of the evidence.

8. Patent Owner's Motion to Exclude Evidence (Paper 58)

Patent Owner seeks to exclude the declaration testimony of Dr. Foty (Exs. 1003, 1029) on the ground that Dr. Foty "lacks even ordinary skill in the art." Paper 58, 1. We need not reach this motion, because even assuming that Dr. Foty possesses at least ordinary skill in the art we determine that Petitioner has not proved by a preponderance of the evidence

that any challenged claim is unpatentable. Thus, we dismiss Patent Owner's motion to exclude as moot.

9. Petitioner's Motion to Exclude Evidence (Paper 59)

By this motion, Petitioner seeks to exclude paragraphs 136 and 138–144 of Exhibit 2008, and Exhibits 2018, 2021–2043, 2047, 2049, 2051, 2052, and 2054. Paper 59, i.

Paragraphs 136 and 138–144 of Exhibit 2008, and Exhibits 2018, 2021–2043, 2047, 2051, and 2052 all pertain to Patent Owner's arguments regarding secondary considerations of nonobviousness. Given that Petitioner has failed to prove obviousness of any challenged claim even before assessing any objective evidence of nonobviousness presented by Patent Owner, we need not and do not consider paragraphs 136 and 138–144 of Exhibit 2008, and Exhibits 2018, 2021–2043, 2047, 2051 and 2052. Thus, we dismiss Petitioner's motion to exclude this evidence as moot.

Exhibit 2049 is a journal article.[14] When making its objection to the exhibit, Petitioner stated: "Petitioner objects that this exhibit lacks proper authentication. Petitioner further objects on the grounds of hearsay, relevan[ce], and F.R.E. 403." Paper 35, 5.

Regarding alleged lack of proper authentication, Patent Owner explains:

> Exhibit 2049 is a technical article regarding leakage current in NMOS and PMOS transistors "published in [a] peer-reviewed professional publication[]" i.e., the Journal of Applied Physics—an established journal that "provide[s] specific publication numbers, printing dates and publisher information, all of which

[14] C.T. Angelis, et al., *Study of Leakage Current in n-channel and p-channel Polycrystalline Silicon Thin-Film Transistors by Conduction and Low Frequency Noise Measurements*, 82 J. Appl. Phys. 4095 (1997).

> are indicia understood, at least under Rule 902(6), as characteristics of self-authenticating documents," and is thus "self-authenticating under Federal Rule of Evidence 902(6)."

Paper 61, 12. Petitioner provides no corresponding rebuttal. We agree that Exhibit 2049 is a self-authenticating document for the same reasons mentioned by Patent Owner.

Exhibit 2049 is also not irrelevant. It is underlying material on which Patent Owner's expert, Dr. Wolfe, relies on for his opinion that one of ordinary skill in the art would have understood that there were other meaningful differences between nMOS and pMOS transistors. *See* Ex. 2008 ¶ 63. Furthermore, Petitioner does not provide explanation of why Exhibit 2049 fits this description of excludable relevant evidence: "The court may exclude relevant evidence if its probative value is substantially outweighed by a danger of one or more of the following: unfair prejudice, confusing the issues, misleading the jury, undue delay, wasting time, or needless presenting cumulative evidence." Fed. R. Evid. 403. We are not persuaded that Exhibit 2049 should be excluded under Rule 403.

Regarding hearsay, Petitioner has not identified any particular statement within Exhibit 2049 for evaluation of the hearsay question. For that reason alone, the motion lacks merit regarding the assertion of hearsay. Further, the following constitutes a hearsay exception: "A statement in a document that was prepared before January 1, 1998 and whose authenticity is established." Fed. R. Evid. 803(16). Patent Owner notes that Exhibit 2049 has a publication date of October 15, 1997, and thus falls within the ancient documents exception of Rule 803(16). Paper 61, 13. Petitioner provides no corresponding rebuttal. We agree with Patent Owner that the hearsay exception under Rule 803(16) applies. In addition, we note further

that the facts and data on which Dr. Wolfe relies to formulate his opinion need not themselves constitute admissible evidence. Fed. R. Evid. 703. Petitioner has not shown any prejudicial effect of Exhibit 2049 that outweighs its probative value. *See id.*

Exhibit 2054 is an Order from the Administrative Law Judge in related ITC proceeding finding "that Dr. Foty does not meet the level of ordinary skill in the art for the '599 and '593 patents . . . ." Ex. 2054, 5. We need not reach Petitioner's Motion to Exclude as it relates to Exhibit 2054 because, as noted above, even assuming that Dr. Foty possesses at least ordinary skill in the art, we determine that Petitioner has not proved by a preponderance of the evidence that any challenged claim is unpatentable.

For the foregoing reasons, Petitioner's Motion to Exclude is *denied* with respect to Exhibit 2049, and *dismissed* with respect to Paragraphs 136 and 138–144 of Exhibit 2008, and Exhibits 2018, 2021–2043, 2047, 2051, 2052, and 2054.

10. Petitioner's First Motion to Strike (Paper 37)

Petitioner filed a Motion to Strike directed to portions of the Patent Owner Response which allegedly incorporate by reference material from Exhibits 2018, 2047, 2051, and 2052. Paper 37. Patent Owner filed an opposition to that motion (Paper 38) and Petitioner filed a reply (Paper 39).

Exhibits 2018, 2051, and 2052 are claim charts mapping challenged claims to respective device. They are relied on by Patent Owner in connection with Patent Owner's presentation of objective evidence of nonobviousness. PO Resp. 54–55, 60–61. Exhibit 2047 is the Complaint in related civil action *Samsung Display Co., Ltd. v. BOE Technology Co., Ltd.*, Case No. 2-23-cv-00309 (E.D. Tex.). Patent Owner relies on paragraphs

31–50 of the Complaint to support its assertion of copying by Petitioner as objective evidence of nonobviousness. PO Resp. 59–60.

We need not reach this motion because, as explained above, in the circumstances of this case we need not and have not considered Patent Owner's objective evidence of nonobviousness.

11. Petitioner's Second Motion to Strike (Paper 46)

Petitioner filed a Second Motion to Strike directed to arguments in Patent Owner's Sur-reply and Exhibit 2054 cited therein. Paper 46. The arguments sought to be stricken are those which assert that Dr. Foty, Petitioner's expert, lacks even ordinary skill in the art. "Petitioner is moving to strike Patent Owner's evidence (EX2054) and related argument that Dr. Foty does not **qualify as a POSITA**." *Id.* at 2 (emphasis in original).

We need not reach this motion, because even assuming that Dr. Foty possesses at least ordinary skill in the art, we determine that Petitioner has not proved by a preponderance of the evidence that any challenged claim is unpatentable.

III. CONCLUSION

We determine that Petitioner has not proved by a preponderance of the evidence that any of claims 1–18 of the '599 patent is unpatentable.

In summary:

Claims	35 U.S.C. §	References/Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
1–18	103	Kimura		1–18
Overall Outcome				1–18

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–18 of the '599 patent have not been proved unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Exclude (Paper 58) is *dismissed*;

FURTHER ORDERED that Petitioner's Motion to Exclude (Paper 59) is *denied* with respect to Exhibit 2049, and *dismissed* with respect to paragraphs 136 and 138–144 of Exhibit 2008, and Exhibits 2018, 2021–2043, 2047, 2051, 2052, and 2054;

FURTHER ORDERED that Petitioner's First Motion to Strike (Paper 37) is *dismissed*;

FURTHER ORDERED that Petitioner's Second Motion to Strike (Paper 46) is *dismissed*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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